A simple delay-line 4-PPM demodulator with near-optimum performance

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Abstract: We describe a simple 4-PPM demodulator that uses analog delay lines and simple 1-bit comparators to determine the least-significant bit and most-significant bit of the 4-PPM encoded data without additional digital signal processing. We show that with good optical filtering the comparator-based demodulator can theoretically operate with sensitivity only 0.23 dB from the optimum 4-ary receiver. We describe as an example of this approach the demodulator built for the Lunar Laser Communication Demonstration and show measured performance within 1.1 dB of the expected sensitivity. The technique is extendable to higher-order, and higher-symbol-rate orthogonal modulation formats.

OCIS codes: (060.2605) Free-space optical communication; (060.4510) Optical communications; (060.4080) Modulation.

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Introduction

M-ary Pulse-position modulation (*M*-PPM) is an attractive format for power-constrained optical communication. 4-PPM has nearly the sensitivity of DPSK but does not require a stable interferometer locked to the signal wavelength. *M*-PPM like all orthogonal modulations provides its own decision threshold and thus can operate with high performance even with rapidly varying signal powers. Channel fading from atmosphere-caused scintillation on an uplink received signal can be mitigated by a single *M*-PPM optical receiver in space with non-coherent combining of a multi-carrier spatial-diversity transmitter on the ground.

Satellite receivers must also make efficient use of electrical power as well as requiring high photon efficiency constraining the digital signal-processing power available on the satellite. For these reasons there has been recent interest in developing high-sensitivity, low-power, low-complexity, *M*-PPM demodulator solutions for space applications [1–3].

The demodulator described here uses an analog delay approach and simple 1-bit comparators to determine the least-significant bit (LSB) and most-significant bit (MSB) of the 4-PPM encoded data without additional digital signal processing. We show that with good optical filtering the comparator-based demodulator can theoretically operate with sensitivity only 0.23 dB from the optimum 4-ary receiver. We describe as an example of this approach the demodulator built for the Lunar Laser Communication Demonstration (LLCD) and show measured performance within 1.1 dB of the expected sensitivity. The technique is extendable to higher-order, and higher-symbol-rate orthogonal modulation formats.

Comparator-based demodulator design

The optimum *M*-ary orthogonal receiver has a matched filter for each transmitted symbol and measures the total signal and noise power at the output of each filter for every symbol interval. The demodulator then chooses the largest output as the transmitted symbol. This can be implemented by *M* multi-bit analog-to-digital converters (ADC) operating at the symbol rate. Satellites are very power limited and multiple high-speed ADC's can require a significant amount of power. In the case of pulse-position modulation (PPM) a single ADC can be used but the sampling rate increases to the PPM slot rate. The digital electronics performing the "pick max" comparison following the single ADC must also process multiple bits of data at the PPM slot rate.

M-ary orthogonal modulations can be demodulated, with near-optimum performance, using simple 1-bit comparators operating at the symbol rate [4]. This is accomplished by combining multiple symbol matched-filter outputs in the analog domain and making simple 1-bit comparisons of the combined outputs. This concept is generalized in Fig. 1 (a) for 4-ary orthogonal modulations.

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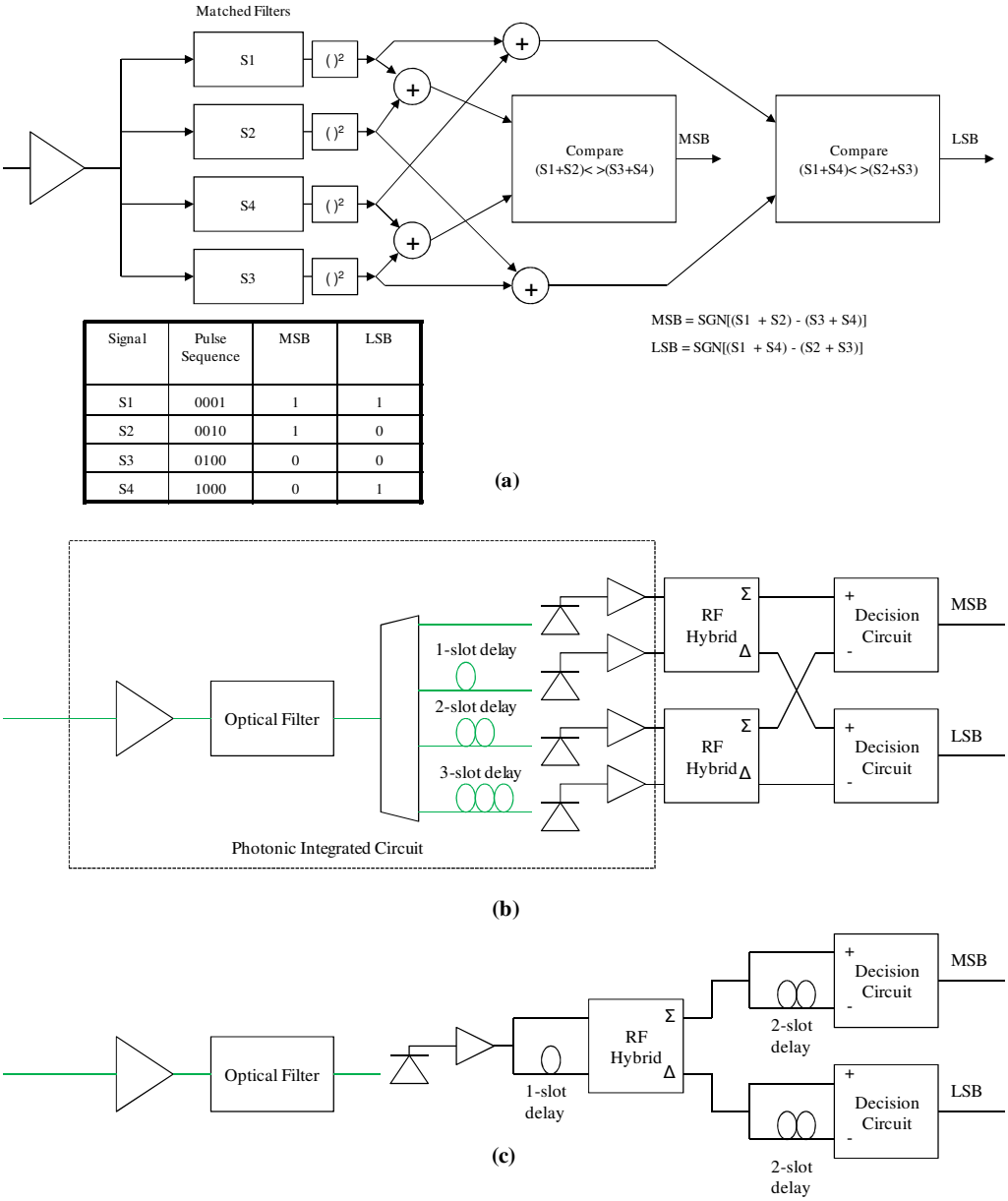

Signal	Pulse Sequence	MSB	LSB
S1	0001	1	1
S2	0010	1	0
S3	0100	0	0
S4	1000	0	1

Fig. 1. Comparator-based demodulation of 4-ary orthogonal signaling. (a) Generalized 4-ary orthogonal demodulation with post-detection combining of matched-filter outputs. The mapping of data bits to pulses used for the LLCD 4-PPM demodulator is shown. (b) 4-PPM demodulator implementation with optical delays and post-detection combining. (c) 4-PPM demodulator implementation using a single optical detector and post-detection combining with electrical delays (used for LLCD).

The signal with symbols S1 through S4 is sent to a set of filters labeled S1 through S4, each of which is matched to that particular symbol. The envelopes of the filter outputs are generated using square-law detection, e.g. a photo-diode for optical systems. The bandwidth of the detectors must be large enough to pass the PPM pulse envelope. These signals are then combined following the detectors as shown and compared using simple 1-bit comparators (decision circuits) to generate the demodulated data.

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For the particular case of PPM, since the orthogonality is in time, not frequency, all of the symbols can make use of a single, matched pulse filter up front followed by delay lines that provide time discrimination of the symbol pulses. The location of the delay lines is an implementation choice. Optical delays can be used in the position of filters S1 through S4 before each of the photo-detectors with post-detection combining as shown in Fig. 1 (b). The implementation could use photonic-integration at high data rates as proposed for similar architectures [5–8]. Our approach, described in detail in the following section, uses an optical filter followed by a single photo detector with electrical delay lines and combiners shown in Fig. 1 (c). We chose this implementation for simplicity at lower data rates.

The mapping of bits-to-symbols, shown in Fig. 1 (a), provides a simple Gray code [9] such that an error caused by leakage of signal into nearest-neighbor filters results in at most 1 bit error. This mapping was chosen for the Lunar Laser Communication Demonstration (LLCD) 4-PPM demodulator described in the following section.

There is a small penalty in performance using this type of demodulator over the optimum receiver because each comparison has two modes instead of one in the ideal receiver, where the modes are defined as the dimensionality of the signal space in time and frequency [10]. The performance is degraded as if we built a "pick maximum" receiver but used filters that had twice the optimum noise bandwidth. Humblet [11] analyzed binary FSK systems with non-optimal filters. Humblet's analysis is valid for all binary orthogonal modulations and we can apply it to *M*-ary orthogonal systems built with the simple comparator demodulator shown in Fig. 1 because each bit decision is an independent binary comparison of signal-plus-noise to noise. We have only to account for the multiple modes due to the combining (doubling in the case of 4-ary), and that we are sending multiple bits instead of one with every symbol.

Humblet's formula for probability of error for the binary case is shown in Eq. (1):

$$P_e = \frac{1}{2^N} e^{-\frac{E}{2N_o}} \sum_{k=0}^{N-1} c_k \left(\frac{E}{2N_o} \right)^k , \tag{1}$$

where $c_k = \frac{1}{k!} \sum_{i=k}^{N-1} 2^{-i} \binom{N+i-1}{i-k}$.

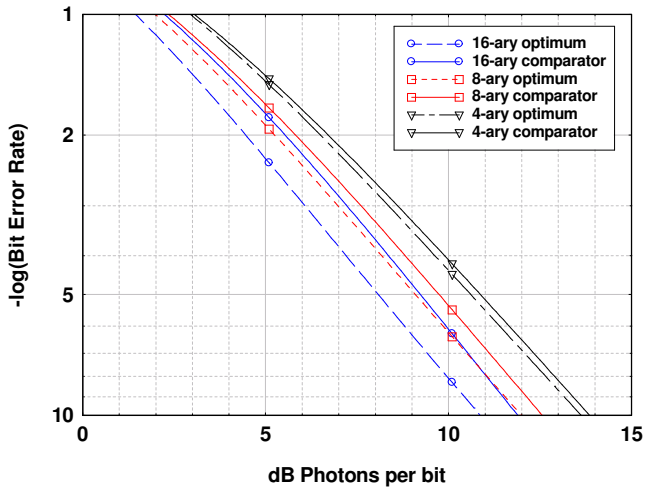

Fig. 2. Optimum and comparator-based receiver performance for M-ary orthogonal modulation. Solid curves show comparator-based receiver performance. Dashed curves show optimum demodulator performance. 16-ary = blue circles, 8-ary = red squares, 4-ary = black triangles.

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E/N_0 is the signal-to-noise ratio which for a pre-amplified optical receiver is the number of photons-per-bit at the input to an ideal high-gain optical amplifier. We have used N as the number of modes, replacing M in Humblet's formula to avoid confusion with the alphabet size of the M-ary modulation. N is given by $2N = 2BT + 1$, where B is the optical bandwidth and T is the pulse duration. For an ideal, single-polarization receiver with a matched filter $N = 1$, and the formula reduces to the well known result for binary orthogonal modulation. A receiver that passes both polarizations has double the modes of a single-polarization receiver. The comparator-based demodulator described here multiplies the number of modes by $M/2$, doubling the number of modes again in the 4-ary case and quadrupling the number of modes for an 8-ary modulation. Although the receiver sensitivity degrades as the number of modes increases, the comparator-based demodulator can achieve near-optimum performance for 4-ary modulations with good optical filtering.

Observing that the comparator-based demodulator makes independent binary measurements, one for each bit, we make use of Eq. (1) by interpreting E/N_0 as the number of photons-per-symbol, and P_e as the probability of error for each bit decision. With equally likely transmitted symbols, P_e is the bit-error rate. The photons-per-bit are the (photons-per-symbol)/$\log_2(M)$. Figure 2 plots a comparison of the probability of error for 4-ary, 8-ary, and 16-ary orthogonal modulations with matched filtering, and one polarization for optimum (dashed) and comparator-based (solid) demodulators. The penalty for comparator-based demodulation increases for modulations with larger alphabets and wider optical filters.

The optimum demodulator performance for M-ary orthogonal modulations [12] is plotted in Fig. 2 using Eq. (2):

$$P_e = \frac{M}{2(M-1)} \sum_{k=1}^{M-1} \frac{(-1)^{k+1}}{k+1} \binom{M-1}{k} e^{-\left[\frac{kN_s}{k+1}\right]}. \qquad (2)$$

P_e is the probability of bit error and N_s is the number of photons per symbol. The penalty is shown to be about 0.23 dB from the optimum receiver performance for 4-ary modulation with good filtering at 10^{-2} bit-error rate.

The modes are increased with wider-than-optimum optical filtering. Wide filtering might be used at low data rates where narrow filters are impractical or unavailable, to allow for optical carrier drift, or to accommodate multiple optical carriers (as in our case) to mitigate fading. Equation (1) was used to calculate the performance over a wide range of modes. Figure 3 shows the expected performance of a 4-ary comparator-based demodulator for 2–220 modes. Ideal DPSK theory is shown for reference.

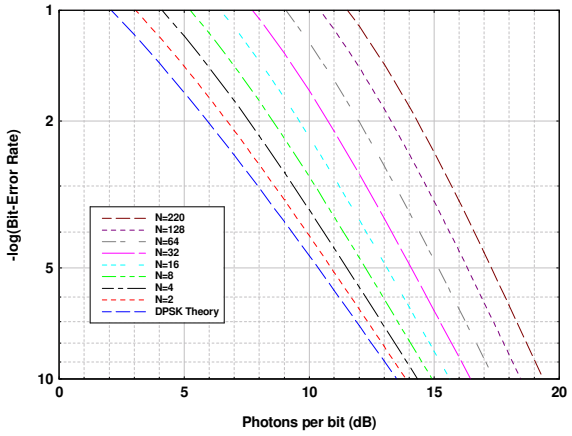

Fig. 3. 4-ary comparator-based receiver performance. N is the number of modes given by ($2N = 2BT + 1$) x (number of polarizations) x 2.

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Lunar laser communication demonstration 4-PPM demodulator

The Lunar Laser Communication Demonstration (LLCD) will provide bi-directional laser communication links between the earth and the Lunar Atmosphere and Dust Environment Explorer (LADEE) satellite orbiting the moon [13, 14] with the launch scheduled in 2013. The downlink uses 16-PPM modulation at 1550 nm with a transmitter power of 0.5 W and a maximum information rate of 622 Mbps. The downlink receiver uses an array of superconducting single-photon detectors. The uplink uses 4-PPM variable-duty-cycle modulation [15] to provide 9.72 and 19.44 Mbps information rates with a pre-amplified, direct-detection, comparator-based demodulator receiver on-board the satellite. Mitigation of atmosphere-caused scintillation on the uplink received signal is accomplished by sending four optical carriers from the ground terminal with each carrier on a separate optical telescope separated by greater than the turbulence correlation distance and non-coherently combined at the receiver photo detector. The optical carriers are separated by approximately 1 GHz to move the coherent mixing products outside of the post-detection electrical filter pass-band [16]. The optical receiver bandwidth was selected to be 10 GHz to easily accommodate the four carriers plus provide additional bandwidth for Doppler and filter temperature drifts.

The LLCD space terminal is highly constrained in terms of size, weight, and power. A demodulator design was needed that would minimize the signal processor requirements on the satellite and yet provide good photon efficiency. A 4-PPM modulation format was chosen to provide receiver sensitivity close to that of DPSK while accommodating multiple optical carriers in a single receiver with relaxed specifications on uplink wavelength settings. Both uplink and downlink use rate-1/2 turbo coding and channel bit interleaving for forward error correction (FEC) in the fading channel.

The uplink 4-PPM modulation format is shown in Fig. 4 where the transmitted symbols have 4-PPM modulation in the first four slots and an additional 12 (19.44 Mbps) or 28 (9.72 Mbps) slots of dead time where no transmitter power is sent. An average-power-limited EDFA-based master-oscillator-power-amplifier (MOPA) architecture increases the peak power of the lower data rate signal. This modulation format allows the receiver demodulator to accommodate multiple data rates with a single filter and clock recovery system [15,17].

Fig. 4. LLCD uplink PPM waveforms.

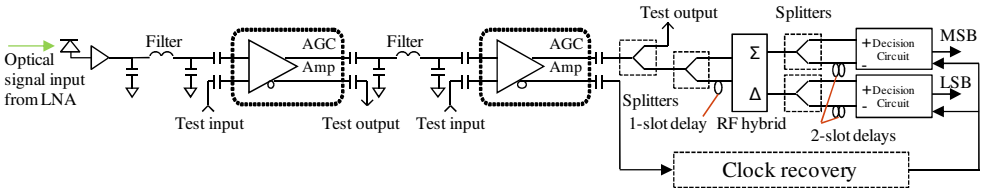

Fig. 5. LLCD 4-PPM demodulator design.

The 4-PPM demodulator design shown in Fig. 5 is based on the block diagram in Fig. 1 (c). The design is an extension of a previously-demonstrated 2-PPM design [17] with the addition of two more delay lines and one comparator. The demodulator receives pulses from a photo detector and trans-impedance amplifier following a two-stage low-noise amplifier. With wide optical filtering, two stages of electrical filtering are used to filter the signal pulses. Two electrical gain stages provide automatic gain control over a 20-dB optical, 40-dB electrical dynamic range. The two differential output signals from the second-stage amplifier are used separately for signal demodulation and clock recovery. The clock output feeds a phase

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detector for the clock-recovery phase-locked loop. The other signal output is split to provide a test port for waveform monitoring and then splits into two electrical paths with a differential delay of one slot width. These two branches feed an RF 180-degree hybrid power divider. The hybrid sums the two inputs at one output (Σ) and subtracts the two inputs at the other output (Δ) resulting in a doubling of the input pulses. These two outputs are again split into two paths with differential delays of two slot widths. Each pair of output signals feeds the differential inputs of a high-speed comparator (decision circuit) latched by the recovered symbol clock. The comparators, in effect, subtract their two delayed inputs. The comparators are sampled at the appropriate time and output the decisions for the MSB and LSB of the 4-PPM modulated signal. Figure 6 shows the evolution of the 4-PPM pulses as they pass through the demodulator.

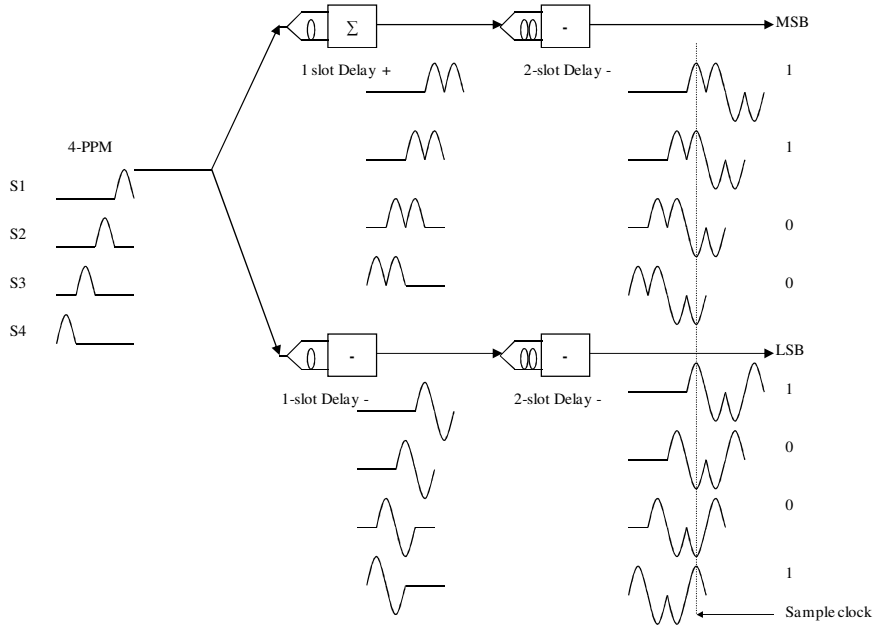

Fig. 6. 4-PPM waveform evolution through the demodulator. The combination of delays, sums, and differences results in an overlay of pulses that provides an unambiguous determination of the transmitted bits when sampled at the appropriate time shown by the sample clock.

The resulting eye pattern at the output of the delay lines and combiners is shown in Fig. 7. The bandwidths of the electrical low-pass filters, shown in Fig. 5, were determined experimentally by minimizing the optical power required for measured bit-error rates in the 10^{-3} to 10^{-2} range. This resulted in a small amount of inter-symbol interference evidenced by some distortion particularly in the LSB waveform. The LSB shows more distortion because the waveform has more high frequency content than the MSB as a result of the difference in pulse patterns.

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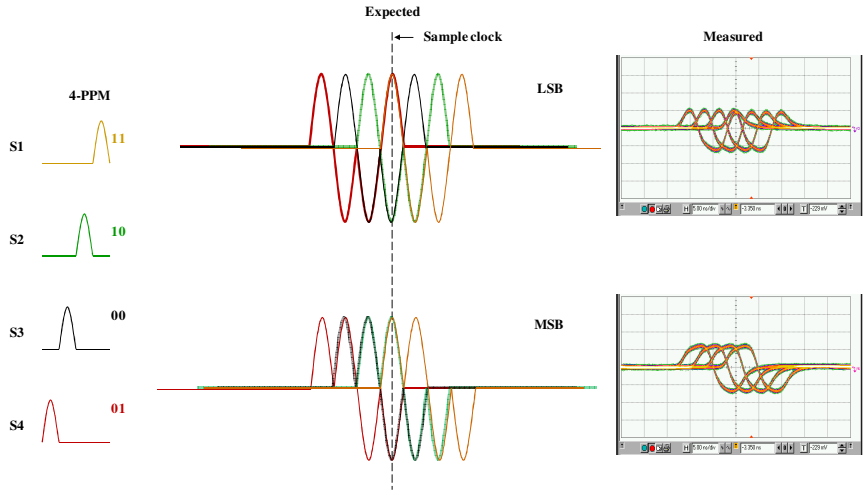

Fig. 7. Expected and measured eye patterns at the demodulator output. The measured eye patterns were generated using a pattern generator at the input to the demodulator and subtracting the LSB + and LSB- and the MSB + and MSB- output waveforms using an oscilloscope. This subtraction would normally occur internally in the comparators.

Clock recovery

The symbol clock recovery uses an analog frequency mixer as a phase detector multiplying the 4-PPM pulse stream and a square-wave clock waveform generated by the local symbol clock on the satellite. The phase detector generates an error voltage that tunes a voltage-controlled oscillator pulling the rising edge of the symbol clock to the point between the second and third slots of the 4-PPM waveform. A single, fixed clock delay then centers the clock edge in the data eye at the comparators for both data rates.

A voltage-controlled surface-acoustic-wave crystal oscillator (VCSO) is used as the master clock at 2.48832 GHz. This oscillator is multiplied up to 4.97664 GHz for the downlink slot clock. It is then divided by 256 or 512 by a combination of the downlink 16:1 serializer, a T-flip-flop, and the FPGA to produce the uplink symbol clocks at 19.44 and 9.72 MHz as shown in the block diagram in Fig. 8.

The phase-locked loop (PLL) operates in two modes determined by the state of a frame-sync flag in the FPGA. When there is no uplink frame sync, the PLL operates in a wide-bandwidth first-order mode allowing the loop to acquire lock over a frequency offset of several hundred parts-per-million (ppm). This is more than adequate to accommodate expected Doppler shifts (7 ppm) and VCSO temperature drifts. The measured VCSO tuning voltage over temperature was fitted to a second-order polynomial equation which is used by the on-board computer to pre-tune the VCSO based on measured temperature and known Doppler prior to clock acquisition.

The FPGA is continually searching for a unique pattern in the coded frame header. When the FPGA recognizes the frame header it asserts the frame-sync flag. The on-board computer in the LLCD controller electronics module then trims the VCSO tuning voltage to minimize the tuning error and switches the PLL to a low-bandwidth second-order tracking mode. Once in the second-order tracking mode the analog integrator in the PLL continues to track the uplink symbol clock over Doppler and temperature drifts. If frame sync is subsequently lost, the loop reverts back to the wide-bandwidth first-order acquisition mode and waits for frame sync to return.

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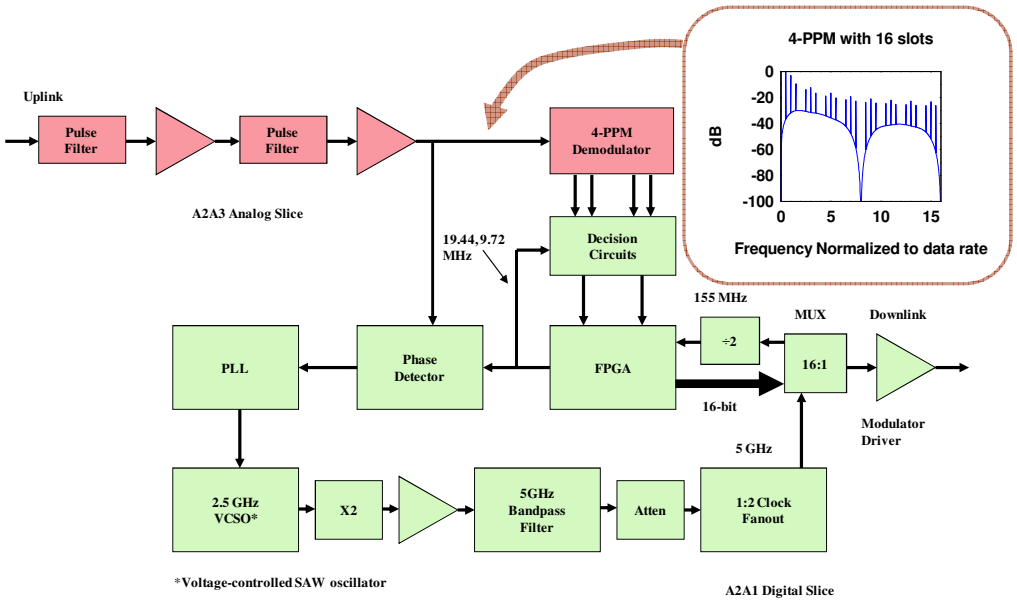

Fig. 8. Block Diagram of the LLCD uplink demodulator and clock recovery. The inset in the upper right shows the 4-PPM spectrum for the higher data rate. The variable-duty cycle format has a strong clock spectral line at the symbol clock rate (half the channel data rate) which is used for clock recovery.

The clock recovery has demonstrated phase locking with frame-sync acquisition at −78 dBm optical power at the input to the receiver low-noise amplifier, about 10 dB below the expected worst case operating signal level. We have also demonstrated clock tracking with a simulated VCSO temperature rise of 3 degrees-per-minute by ramping the uplink 311.04 MHz transmitter slot clock at 167 parts-per-billion (ppb) per second.

Performance

The 4-PPM satellite uplink will use the Serially Concatenated Pulse-Position Modulation (SCPPM) rate-½ turbo code [18] with an error-free decoding threshold at 6 x 10^{-2} channel error rate. The FEC decoding and de-interleaving will be performed by a Virtex-4 FPGA shown in the block diagram in Fig. 8. We present here the channel error-rate performance without coding but we refer to the required optical power at the decoding threshold as the figure-of-merit of interest for this system.

A breadboard version of the low-noise amplifier (LNA) designed for the spacecraft modem [14] was used as the optical front-end. The amplifier is a dual-polarization two-stage design with 20-dB of gain in the first stage and 23-dB of gain in the second stage. The overall noise figure including an isolator at the input is 3.9 dB, i.e. 0.9-dB excess noise. A 0.823-nm (101-GHz) filter follows the first-stage amplifier and a 17-GHz filter follows the second stage. A commercially available PIN-TIA was used as the optical-to-electrical converter.

The test transmitter used a DFB laser at 1563 nm followed by a Lithium Niobate Mach-Zehnder modulator. An optical attenuator was used to simulate channel loss. A 50/50 coupler at the output of the attenuator was calibrated to provide a monitor point to measure optical power at the input to the LNA. The data source was a pattern generator programmed with a 2^7-1 PRS encoded for 4-PPM with either 16 slots or 32 slots for the two uplink data rates.

The PPM slot rate is 311.04 MHz. With the 17-GHz optical filter used in this test, our comparator-based demodulator has 220 modes {55 (*BT*) x 2 (polarizations) x 2 (4-PPM comparator demodulator)}. The measured performance with optical power is shown in Fig. 9.

The receiver sensitivity shows excellent agreement with the expected performance. A bit-error rate of 6 x 10^{-2} was achieved with optical signal powers of −72.5 dBm and −69.5 dBm

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at 19.44-Mbps and 38.88-Mbps channel rates respectively. Figure 10 compares the measured performance in photons-per-channel-bit to the theory for N = 220 modes. With an ideal receiver noise figure, the demodulator is expected to operate error free with coding at 12.4-dB photons-per-channel bit or −73.6 dBm at 19.44-Mbps channel rate and −70.6 dBm at 38.88-Mbps channel rate. The 1.1-dB offset from ideal performance is largely accounted for in the measured excess noise figure of 0.9 dB for the low-noise receiver amplifier used in this test.

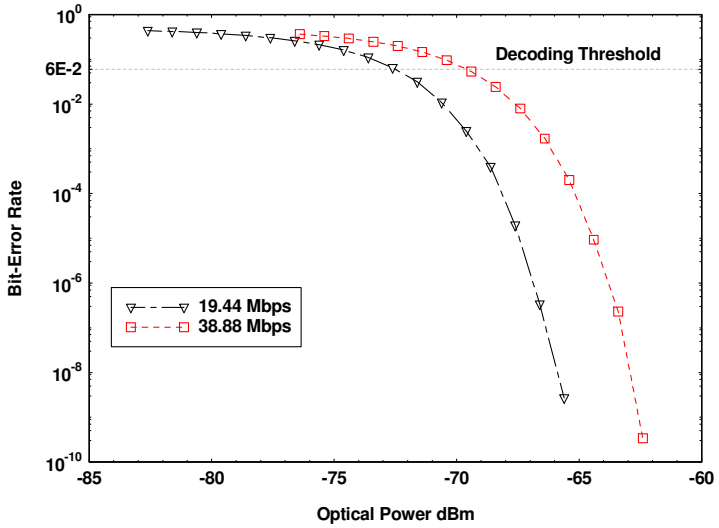

Fig. 9. Channel bit error rate without coding vs. optical power. 19.44 Mbps (black triangles), 38.88 Mbps (red squares). The decoding threshold for a coded system is shown for reference only.

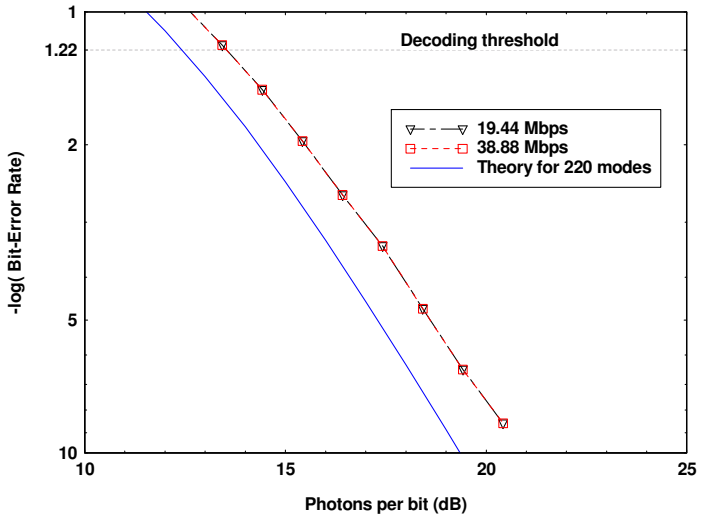

Fig. 10. Measured channel error rate performance without coding compared to theory for a comparator-based 4-PPM demodulator with 220 modes. The decoder threshold for a coded system is shown for reference only.

A similar demodulator approach was reported by Caplan [19] for an 8-ary FSK system where the outputs of multiple optical filters are combined before the photo detectors. The performance of this system also appears to be in good agreement with the theory presented here.

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Conclusions

A simple 1-bit-comparator-based 4-ary orthogonal demodulator is shown to perform within 0.23 dB of the optimum receiver. The comparator-based design requires no additional signal processing following the demodulator providing potential power savings over the optimum receiver implementation. The hardware design and performance of a 4-PPM comparator-based demodulator developed for the Lunar Laser Communication Demonstration provides validation of this approach with measured performance within 1.1 dB of the expected sensitivity. The comparator-based design has been shown to be extendable to higher-order *M*-ary orthogonal modulation formats and higher symbol rates.

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