Packet-level synchronization scheme for optical packet switched network nodes

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Abstract: We demonstrate an all-optical, self-synchronization scheme for optical packet switched network nodes. It provides both the packet clock signal and the packet beginning, marker pulse. The circuit uses two hybridly integrated MZI switches and has been evaluated with synchronous, asynchronous and variable length, data packets at 10 Gb/s. It is compact and requires relatively low energies to operate.

OCIS codes: (060.4510) Optical communications; (230.1150) All-optical devices; (250.5980) Semiconductor Optical Amplifiers; (050.2230) Fabry-Perot.

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1. Introduction

Circuits to provide packet-level and bit-level synchronization are essential for the control of optical signal processors in packet switched networks. Packet-level synchronization can be achieved by extracting the first pulse of incoming data packets and is needed to trigger, on a per packet basis, controlling and routing circuits. Bit-level synchronization can be performed with an optical clock recovery circuit [1] and is required for bit-wise processing and 3-R regeneration purposes [2]. So far, several schemes for first pulse extraction have been demonstrated, mainly employing a marker pulse at the beginning of the packet. These approaches require the marker pulse to be at a different state relative to the rest of the packet in terms of wavelength [3], polarization [4], bit period [5] or amplitude [6], resulting in increased transmitter and transmission-link complexity. In order to achieve self-synchronization even when all the data pulses share the same physical state, semiconductor optical amplifier (SOA)-based devices have been proposed, suggesting the exploitation of the bit-level differential SOA gain and phase dynamics [7-10]. However, these techniques require the use of SOAs with very long recovery time in order to operate successfully, leading in this way to high-pattern dependence, which in turn imposes the need for strict line coding schemes and specific packet formats.

In this communication we demonstrate a novel method for all-optical packet-level synchronization. It comprises of a packet clock recovery circuit [1] to provide the packet clock signal and an optical AND gate to extract the first pulse of the packet identifying its beginning. The clock recovery module employs a fiber Fabry-Pérot Filter (FFP) and a commercially available hybridly integrated MZI [11]. First pulse extraction is performed in a following MZI switch in which the incoming packet is logically ANDed with the locally generated packet clock signal delayed by a single bit, as shown in Fig. 1. In this way the first pulse appears in the unswitched port (U) of the MZI and is separated from the rest of the packet which appears in its switched port (S). The circuit has been evaluated with 10 Gb/s PRBS 2^7-1 synchronous and asynchronous data packets of variable length. It retains the features of fast clock capture of the previously demonstrated packet clock recovery circuit [12] and can be employed as front-end to an optical packet-switched node, to provide bit- and packet synchronization signal for data regeneration and packet routing.

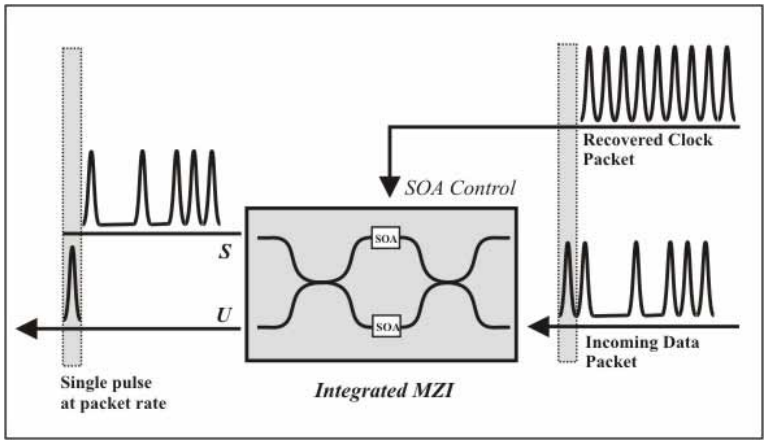

Fig. 1. Schematic of synchronization for first pulse extraction in 2nd MZI

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2. Experimental setup

The experimental setup is shown in Fig. 2. It consisted of a 10 Gb/s optical packet generator capable of generating synchronous and asynchronous packet flows, the packet clock recovery and the first pulse extraction circuits. The input signal was generated by a DFB laser diode (LD 1) at 1549 nm, gain switched at 10.229 GHz to provide 10 ps pulses after linear compression. This pulse-train was modulated into data packets containing PRBS sequences, using a programmable pattern generator and a Ti:$LiNbO_3$ modulator. Asynchronous packet generation could be produced in the packet multiplexer and fine phase adjustment could be achieved with a variable optical delay line in one of the paths of the multiplexer. The generated data packet signal was divided in two parts, one inserted in the packet clock recovery module and the other used in the first pulse extraction unit. The clock recovery circuit employed a fiber Fabry-Pérot Filter (FFP) with free spectral range equal to the line rate and finesse of 47 and an integrated Mach-Zehnder Interferometer (MZI 1) powered by a CW signal at 1555 nm (LD 2), operating as a holding beam [1]. The FFP filter acts as a passive optical resonator that extracts the line rate spectral components of the input signal. The exponentially decaying impulse response of the filter converts the incoming data packets into clock packets with intense pulse amplitude modulation and duration that is similar to that of the incoming packets. This signal was fed into MZI 1 which was saturated by the injection of the CW light and yielded a hard-limiting power transfer function [13] reducing the intensity modulation and providing a good quality packet clock signal. A push-pull configuration was adopted in order to reduce the switching window of MZI 1 to 12.5 ps. MZI 2 was configured as an AND gate to extract the first pulse of the packets to its U-port, using the packet clock as control signal. A single control operation was adopted in MZI 2, since there was no need for bit per bit processing in order for the first pulse extraction to be performed. All the data bits which are logically ANDed with the respective clock pulses are switched irrespective of the SOA recovery time, since all these bits fall within the switching window opened by the packet clock signal envelope. Synchronization between the push-pull signals in MZI 1 as well as between the packet clock control signal and the incoming data packet in MZI 2 was achieved by means of tunable optical delay lines. The SOAs in the MZIs could provide up to 22 dB small-signal gain in the 1547–1557-nm region with 80 ps recovery time, when driven with 270-mA current. Finally the experimental setup included three existing 16 dBm EDFAs to compensate for interconnection losses and 1 nm band pass filters at the output of each MZI to remove the out-of-band SOA noise.

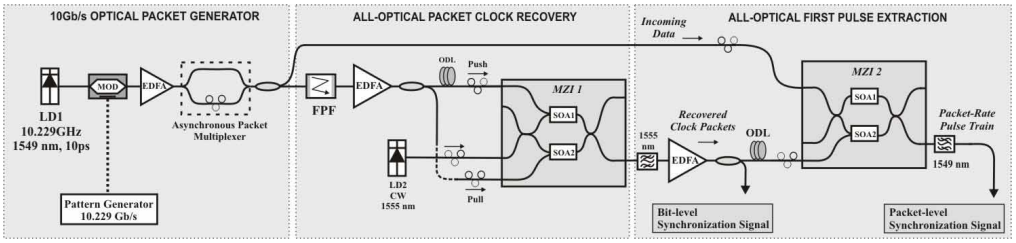

Fig. 2. Experimental Set-up

3. Results and discussion

Packets of unequal, variable and even short length were used synchronously and asynchronously to evaluate the circuit. Typical results for synchronous and asynchronous operation are shown respectively in the left and right columns of Fig. 3. In these examples, for synchronous operation the pattern generator was programmed to generate two consecutive packets of 40 bits and 134 bits, containing a 2^7-1 PRBS data pattern and repeating every 24.83 ns, a period equivalent to a packet rate of 40.27 MHz. For asynchronous operation the packet rate was halved and the packets were interleaved in the asynchronous packet multiplexer. The packet clock recovery circuit sets the requirements for packet formatting and this was

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programmed in the packet generator. With the FFP used, the clock recovery circuit requires 2 consecutive '1s' at the beginning of each packet to acquire clock and decays within 15 bits. The clock capture and decay times set the bandwidth overhead in our packet and bit-level signal synchronization scheme. Figure 3(a) depicts the leading part of the 134 bit input data packet from the synchronous packet sequence and a sequence of two asynchronous packets. Figure 3(b) shows the corresponding recovered clock packets at the output of MZI 1. Best operation of the clock recovery MZI gate was achieved with 790 μW of optical power from the CW source, 200 fJ/pulse for the push and 178 fJ/pulse energy for the pull control signal. Figure 3(c) and 3(d) show the corresponding extracted first pulse(s) synchronization signals and the respective eye-diagrams at the output of MZI 2. The extinction ratio at MZI 2 between the extracted pulses and the following packet bits was in excess of 10 dB and the circuit required 22 fJ/pulse for the incoming data packets and 80 fJ/pulse for the clock packet control signal.

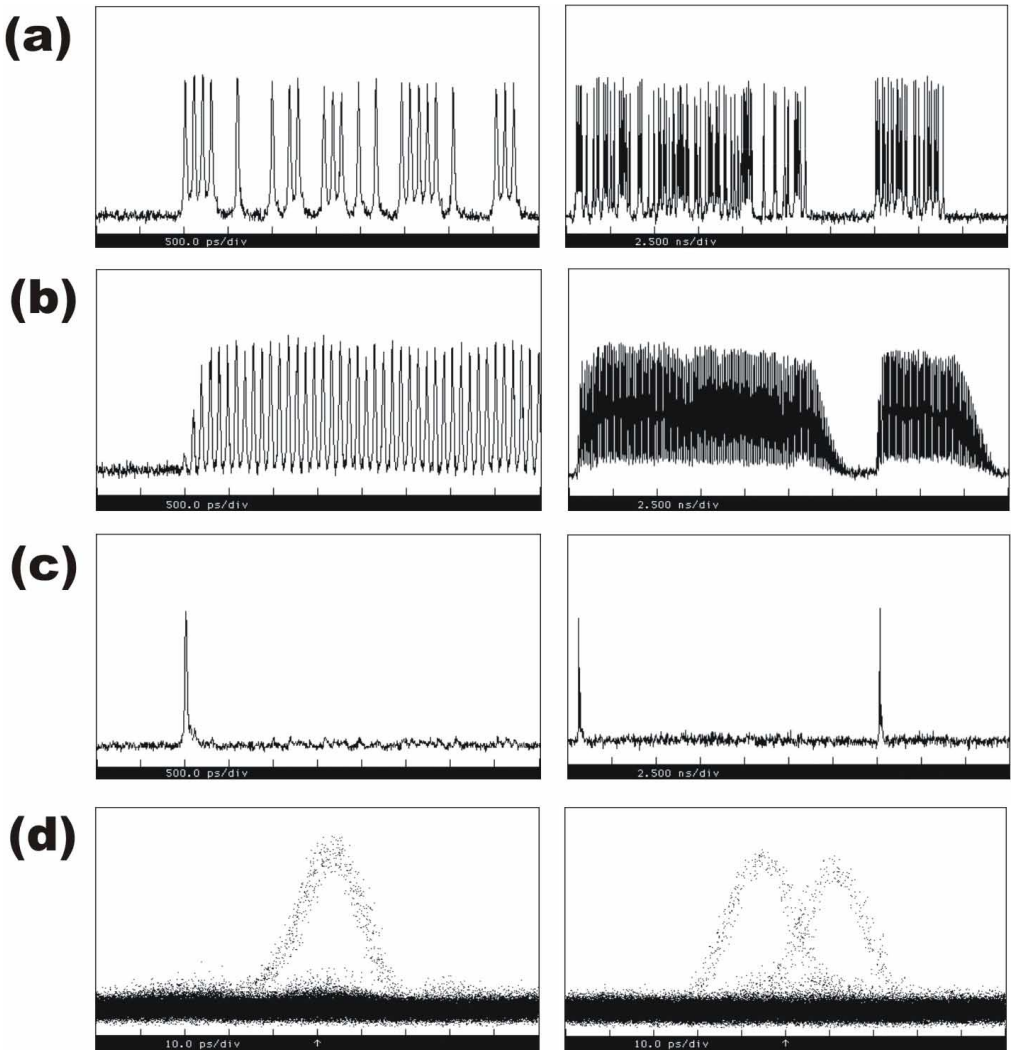

Fig. 3. Oscilloscope traces. Left column: synchronous operation (time scale 500 ps/div), right column: asynchronous operation (time scale 2.5 ns/div). (a): input data packets, (b): recovered clock packets, (c): packet-rate synchronization pulse stream and (d): eye diagrams (time scale 10 ps/div).

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It should be noted that the bandwidth overhead imposed by the circuit is mainly determined by the packet clock rise and decay time. These stem from the filter's finesse, which in turn must be optimized in terms of the expected number of consecutive '0's included in the data signal [1]. For higher than 2^7-1 order PRBSes a filter with higher finesse would be required [1] leading also to an increase in the number of consecutive '1s' at the beginning of each packet. In order to keep these two values low even for higher order PRBS sequences, additional '1' bits have to be included in the sequence, whose role will be to fill in the consecutive '0's PRBS regions with pulses. This is a commonly used technique known as scrambling [14]. In this respect, the filter's finesse and the number of preamble bits will continue to be low, allowing the successful operation of the circuit. However, even in the case where a FFP with high finesse has to be used, the guardband requirements are relative small compared to other electronic or optical clock recovery approaches. As such, the proposed packet-level synchronization scheme fully exploits the fast characteristics of the clock extraction circuit and provides both a packet clock signal and a packet beginning marker pulse without increasing the guardbands needed for just the clock recovery process. Moreover, the total bandwidth overhead imposed by our circuit decreases as the packet length increases [15], since the sum of the packet clock rise and decay time is irrespective of the incoming packet length. Given also that the satisfactory jitter performance of the clock packets demonstrated in [16] renders it suitable for 3R data regeneration, the demonstrated bit- and packet-synchronization circuit forms a promising solution for the implementation of the front-end unit in a packet switched node.

4. Conclusion

In conclusion we have presented a novel all-optical method to derive packet and bit synchronization signals for data packets. Our technique employs a fiber Fabry-Pérot Filter and a hybridly integrated Mach-Zehnder interferometer to implement the packet clock recovery circuit and an additional hybridly integrated MZI to generate single pulses at the leading edge of each incoming packet. The system was shown to operate for variable length synchronous and asynchronous data packets, imposing short inter-packet guard bands.

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