Experimental demonstration of real-time 3Gb/s optical OFDM transceivers

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Abstract: Real-time optical orthogonal frequency-division multiplexing (OOFDM) transceivers based on off-the-shelf components including FPGAs are experimentally demonstrated, for the first time, incorporating key functionalities such as live transceiver optimisation and advanced channel estimation, and also utilising self-developed IFFT/FFT logic algorithms verified at 10Gb/s. The fastest ever real-time end-to-end transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m multi-mode fibers is achieved with BERs of $<3.3\text{x}10^{-9}$ in intensity-modulation and direct-detection systems employing directly modulated DFB lasers. Excellent performance robustness is also observed to various offset launch conditions. This work is a significant breakthrough in demonstrating the great potential of OOFDM for practical implementation in optical networks.

OCIS codes: (060.0060) Fiber optics and optical communications; (060.4080) Modulation; (060.3510) Laser, fiber.

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1. Introduction

Optical orthogonal frequency division multiplexing (OOFDM) [1] has already demonstrated a number of unique and inherent advantages including, for example, great resistance to dispersion impairments, efficient utilization of channel spectral characteristics, potential cost-effectiveness due to full use of mature digital signal processing (DSP), dynamic provision of hybrid bandwidth allocation in both the frequency and time domains, and significant reduction in optical network complexity. As a direct result of the aforementioned features, OOFDM has gained overwhelming research and development interest and, more importantly, is regarded as one of the strongest contenders for enabling the next generation high capacity optical networks required to meet the exponentially growing demand for broadband transmission. Over the past several years, world-wide extensive experimental investigations of the transmission performance of OOFDM of various variants have been reported for all the optical network scenarios including long-haul systems [2,3], metropolitan area networks [4,5] and local area networks [6,7].

However, all the experimental works published previously [1–7] are based on transmission of OOFDM signals originating from arbitrary waveform generators (AWGs) utilising off-line signal processing-generated waveforms. At the receiver, the received OOFDM signals are captured by digital storage oscilloscopes (DSO) and processed off-line to recover the received data. These off-line signal processing approaches do not consider the limitations imposed by the precision and speed of practical DSP hardware required for realizing real-time transmission. Therefore, the experimental demonstration of real-time OOFDM transceivers is critical for not only rigorously validating the OOFDM technique but also establishing a solid platform for evaluating the feasibility of the technique for practical implementation in optical networks.

To implement real-time OOFDM transceivers, highly complex, computationally intense and high-speed signal processing algorithms must be performed in real-time. Although OFDM has already been adopted widely in wireless and wired transmission systems, these systems currently, however, operate at signal bit rates of the order of several tens of Mb/s [8], which are approximately 1000 times lower than those targeted by OOFDM. Thus it is apparent that the real-time signal processing power of an OOFDM system needs to be in the region of three orders of magnitude higher, compared to the existing OFDM-based systems.

The achievement of real-time end-to-end OOFDM transceivers based on real-time DSP with sufficiently high speed and precision is a significant breakthrough in demonstrating the great potential of the OOFDM technique for practical implementation in high capacity optical networks of various architectures. In April 2009, we have reported the world-first implementation of real-time OOFDM transceivers, which support end-to-end transmission of a 1.5Gb/s differential quadrature phase shift keying (DQPSK)-encoded signal over a 500m multi-mode fibre (MMF)-based, intensity-modulation and direct-detection (IMDD) system incorporating a directly modulated DFB laser (DML) [9]. One month later, the real-time OOFDM transmission capacity was doubled, and a transmission of 3Gb/s DQPSK-encoded OOFDM signal over a 500m MMF in the abovementioned transmission system has been successfully demonstrated experimentally [10]. In addition, a real-time OOFDM transceiver incorporating an advanced channel estimation technique proposed by our research group has

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also been implemented, which enables the successful demonstration of 3Gb/s 16-quadrature amplitude modulation (QAM)-encoded real-time OOFDM transmission, in one case, over 75km MetroCor single-mode fibres (SMFs) with negative power penalty in a DML-based IMDD system without in-line optical amplification and chromatic dispersion compensation [10]. Here it is worth addressing that a real-time coherent optical receiver has recently been reported [11], which is, however, not capable of performing end-to-end real-time transmission, as off-line signal processing is still applied in the corresponding transmitter.

In this paper, we report in detail, for the first time, a considerably improved real-time OOFDM transceiver design incorporating a number of newly developed functionalities compared to those reported in [9,10]. Based on the improved transceivers, the fastest ever real-time transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m MMFs with bit error rates (BERs) of $<3.3\text{x}10^{-9}$ has been achieved in DML-based IMDD systems. Excellent performance robustness is also observed to various offset launch conditions. Moreover, transmission performance comparisons are also made between DQPSK- and 16-QAM- encoded 3Gb/s OOFDM signals in the abovementioned transmission systems.

2. Real-time DSP for IFFT/FFT algorithms

2.1 IFFT/FFT algorithms for real-time OOFDM transceivers

OFDM is a multi-carrier modulation technique where a single high-speed data stream is divided into a number of low-speed data streams, which are then separately modulated onto harmonically related, parallel subcarriers. The subcarriers are considered to be orthogonal as their overlapping spectra have the property that they do not interfere at the discrete subcarrier frequencies, thus resulting in high spectral efficiency. At the transmitter, the frequency domain subcarriers must be transformed into a time domain symbol, and at the receiver the time domain symbol must be transformed into the frequency domain subcarriers. As the subcarriers are positioned at equally spaced frequencies, widely used transforms such as the inverse discrete Fourier transform (IDFT) and discrete Fourier transform (DFT) can be adopted. For practical implementation, these transforms are replaced with the more efficient Fast Fourier transform (FFT) and inverse FFT (IFFT) as the computational complexity is significantly reduced. However, for any OFDM-based system, the IFFT and FFT transforms are still the most computationally intense functions, therefore, the real-time implementation of the FFT/FFT algorithms poses one of the greatest challenges for achieving real-time system implementation.

Here, we utilise off-the-shelf field-programmable gate arrays (FPGAs) for real-time hardware-based DSP. We have developed our own custom implementation of a 32 point IFFT/FFT logic function employing a radix-2 decimation-in-time structure comprising of 2-point butterfly elements as the core computational building blocks. To achieve high-speed performance, the IFFT/FFT logic function design is based on a highly pipelined architecture using a number of extensively paralleled processing stages. The custom design permits full control and optimisation of the logic function parameters. The computational precision at each stage of the IFFT/FFT can be controlled to allow the overall calculation precision to be maximised whilst maintaining acceptable logic resource utilisation. In addition, the design can also be scaled to support longer transform lengths required for an increased number of subcarriers, and adapted for higher clock speeds for increased symbol rates. Moreover, the developed IFFT/FFT function also includes adjustable clipping and quantisation of the output samples.

It should be noted that, the developed IFFT/FFT logic function is applicable for all OOFDM application scenarios. Here such a design is applied to an IMDD transmission system of interest in this paper.

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2.2 Evaluation of implemented real-time IFFT/FFT logic functions at 10Gb/s

To evaluate the performance of the developed IFFT/FFT logic designs alone, at 10Gb/s, both the IFFT and FFT functions are implemented in the same FPGA in a back-to-back configuration, as shown in Fig. 1(a). 10Gb/s incoming data is generated externally from a pattern generator. This single data stream is demultiplexed into four 2.5Gb/s streams for input to the FPGA via four high-speed deserialising transceivers. The parallel data from the transceivers is combined and fed to 15 parallel 16-QAM encoders to generate complex data for input to the IFFT logic function. The 15 encoded complex numbers fill the positive frequency bins, and subcarrier 0 corresponding to zero frequency in the electrical domain must be set to zero. For these 16 subcarriers, their 16 complex conjugate counterparts are generated and positioned in the negative frequency bins in such a way that Hermitian symmetry is satisfied between them. This results in the generation of 32 real-valued time domain samples at the output of the IFFT to be compatible with the generation of real-valued signals required in IMDD systems, as discussed in Section 3.

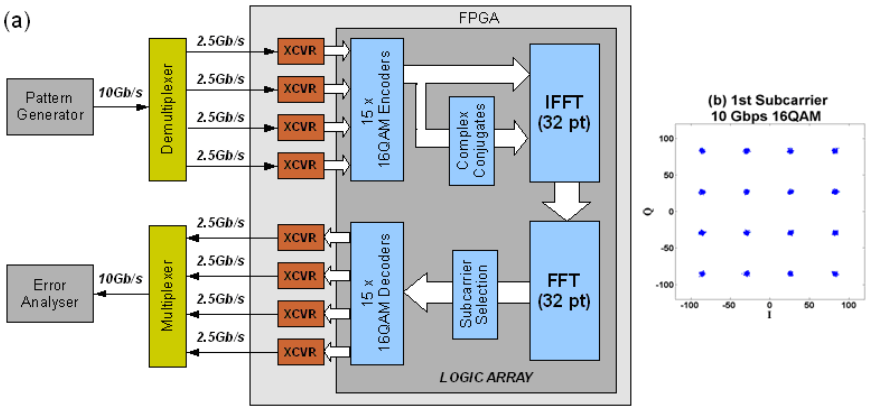

Fig. 1. (a) Experimental system for evaluating IFFT/FFT logic functions; (b) constellation of 16-QAM-encoded first subcarrier after FFT.

These 32 samples from the IFFT function forming an OFDM symbol are clipped and quantised to 8-bits, and are fed directly to the input of the FFT function. From the output of the FFT, the 15 data-carrying subcarriers in the positive frequency bins are selected, which are then decoded by 15 parallel 16-QAM decoders. The resulting parallel data is fed to four high-speed serialising transceivers. The four data streams at 2.5Gb/s are multiplexed to a single 10Gb/s data stream and BER is measured with an error analyser. The FPGA runs at a clock speed of 156.26MHz, which is equal to the symbol rate, as discussed in Section 3.1. The clocks for all the system elements are generated with clock synthesisers using a common reference source.

Zero bit errors are detected by the error analyser at 10Gb/s operation. The constellation of the first subcarrier at the FFT output is shown in Fig. 1(b) and is typical of all subcarriers. This clearly shows that the real-time DSP is capable of supporting at least 10Gb/s OOFDM transmission. It is also estimated that, the use of higher modulation formats, higher clock speeds and more subcarriers can allow the developed IFFT/FFT algorithms to operate at approximately 40Gb/s.

3. Real-time OOFDM transceiver architecture and experimental system

3.1 Real-time transceiver architecture

Figure 2 shows the detailed architectures of the real-time transmitter (top) and the real-time receiver (bottom) developed. The transceiver design has a fully pipelined architecture so that data flow is continuous with very limited buffering of OOFDM symbols. For each OOFDM symbol all samples are processed in parallel.

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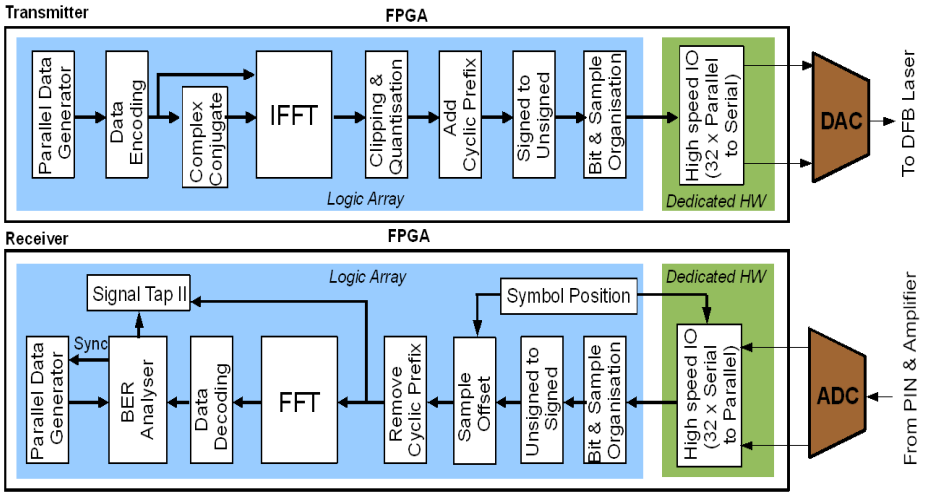

Fig. 2. Real-time OOFDM transceiver architecture.

In the transmitter, a 32 point IFFT is used to support 32 subcarriers, of which 15 carry encoded real data. A parallel pseudo random data source feeds 15 encoders, each of which encodes the data using a specific signal modulation format producing a complex number representing one of the 15 data-carrying subcarriers in the frequency domain. Use is made of these 15 subcarriers to generate 32 real-valued time domain samples, according to the method described in Section 2.2.

After the IFFT, the 32 signed, real-valued samples are clipped and quantized. The number of quantization bits is set to 8, which matches the resolution of the employed DAC. Whilst the clipping ratio can be adjusted, during operation, from a number of preset levels to optimize the transceiver performance. To mitigate the inter-symbol interference (ISI) effect caused by modal dispersion, a cyclic prefix of 8 samples is added to each symbol, giving rise to 40 samples per symbol. The internal system clock is set to be 100MHz, and the parallel processing approach results in a 100MHz symbol rate. The 100MHz symbol rate and 40 samples per symbol give a sample rate of 4GS/s. The relationship between the symbol rate, S, and the signal line rate, R, can be expressed as

$$S = \frac{R}{bN} \tag{1}$$

where b is the number of binary bits encoded on each subcarrier within a symbol, and N is the total number of data-bearing subcarriers in the positive frequency bins. The signed samples are converted to unsigned values by adding an appropriate DC offset, as the DAC requires positive values only. After performing sample ordering and bit arrangement, the unsigned 40 samples are streamed to the DAC interface at 4GS/s. An entire symbol consisting of 320 bits is fed in parallel to 32 high speed 10:1 dedicated hardware serialisers, the interface thus consists of 4 samples transferred in parallel at a rate of 1GHz, giving the required aggregated sample rate of 4GS/s. The DAC generates an analogue electrical OOFDM signal having a maximum peak-to-peak voltage of 636mV. Finally, this signal is used to directly modulate the DML.

At the receiver, after performing optical-to-electrical conversion using a PIN, the analogue electrical signal is digitised by a 8-bit ADC operating at 4GS/s. A digital interface, which is identical to that of the DAC in the transmitter, transfers the digital samples at 4GS/s to the second FPGA. The 32 high speed, 1:10, dedicated hardware deserialisers capture 40 received samples in parallel. Bit rearrangement and sample ordering is also performed to reconstruct

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the samples in the correct order. As required by the FFT function, the samples must be converted to signed values by removing the ADC DC-level code.

Here, symbol alignment is vital to ensure that the 40 parallel samples captured by the deserialisers in the receiver originate from the same symbol generated in the transmitter. Symbol alignment is performed by continuous transmission of symbols of a fixed pattern over the transmission system. By using the FPGA embedded logic analyser (SignalTap II) with JTAG connection to a PC, the captured samples of the fixed symbols can be viewed, thus the sample offset is determined and subsequently compensated by adjusting the inserted sample offset accordingly. It should be pointed out, in particular, that such a symbol alignment process is performed only once at the establishment of a transmission connection.

The first 8 samples of each of the captured symbols are removed, as they correspond to the cyclic prefix added in the transmitter. This leaves 32 samples for input to the 32 point FFT function, which determines the phase and amplitude of each subcarrier. At the FFT output, 15 subcarriers in the positive frequency bins are selected for decoding, subsequently the recovered data bits from each symbol are analysed by a BER analyser function, which regenerates the transmitted bit pattern, synchronises it with the received pattern and continuously detects and counts bit errors.

The bit error count over 100 million symbols is continuously updated and displayed with the embedded logic analyser, this enables fine adjustment of the system parameters to maximize the transmission performance. In addition, the logic analyser also displays and continuously updates the total number of bit errors and the corresponding symbols accumulated since the start of a transmission session. This enables the measurement of BERs at unlimited low values, provided that a sufficiently long operation time is allowed.

For the present demonstration, system clocks for both the transmitter and the receiver are generated from a common reference source. However, it is worth mentioning that, we have developed an advanced technique for clock recovery in the receiver, which, according to simulation results, has sufficiently high accuracy and does not require highly stable and expensive voltage control oscillators. As the thrust of the present paper is to demonstrate experimentally the proof-in-principle of the real-time OOFDM transceivers, the clock recovery technique is, therefore, not implemented in the real-time OOFDM transceivers presented in this paper. The implementation and transmission performance of real-time OOFDM transceivers incorporating clock recovery will be reported elsewhere in due course.

DQPSK signal modulation has the property that no channel estimation is necessary, as data is encoded using differential phase change only. To further improve the transmission capacity, the use of higher signal modulation formats such as M-ary QAM is essential. In M-ary QAM systems, the involvement of both amplitude and phase values means that channel estimation is vital. Very recently, we have developed a novel pilot subcarrier-assisted channel estimation technique [10], which has a number of salient advantages including, for example, high accuracy, low complexity, small pilot bandwidth usage, excellent stability and buffer-free data flow. The detailed operating principles of the technique have been reported in [10], in which rigorous evaluations of the technique have also been made under various operating conditions. In this paper, the channel estimation technique is implemented, and comparisons of the transmission performance are made between DQPSK-encoded and 16-QAM-encoded OOFDM signals at 3Gb/s.

3.2 Transceiver architecture improvements

Compared to the transceiver design reported in [9,10], a number of important new functionalities have been developed, fully verified and incorporated in the transceiver considered. These new functionalities are summarized as followings:

- The FPGA logic design is adapted for clocking at 100MHz (twice the previous speed) to support a doubling of the symbol rate. The sample rate of the DAC and ADC is also increased from 2GS/s to 4GS/s. This is accompanied with a doubling of the data rate of the associated digital interface with the FPGAs. Clearly, these amendments

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improve the operating speed of the OOFDM transceiver by a factor of 2 for a fixed signal modulation format.

- As already mentioned in Section 3.1, the advanced channel estimation technique is implemented, supporting not only the use of arbitrary modulation formats on subcarriers but also live measurements of end-to-end channel frequency responses. This feature enhances significantly the robustness and flexibility of the transceiver, and also provides an effective means for live monitoring of channel quality.
- Live transceiver optimisation. Such property is realised due to the inclusion of the following two new features: a) provision of real-time BERs for all individual subcarriers; b) key transceiver parameters such as signal clipping ratio can be adjusted while the transceiver is still in operation. This feature is very useful for achieving a highly optimised transceiver design for practical implementation.

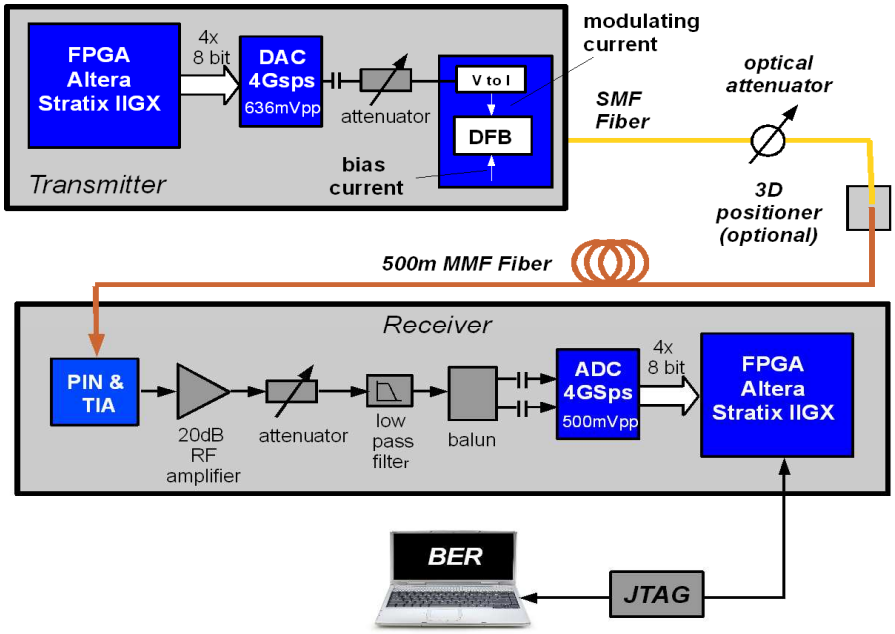

Fig. 3. Experimental system setup.

3.3 Experimental system setup

Figure 3 shows the real-time experimental system setup. The electrical signal from the DAC is first attenuated as required to optimise the modulating current, then it is employed, together with an adjustable DC bias current, to modulate a single-mode 1550nm DFB laser with a 3-dB modulation bandwidth of approximately 10GHz. The OOFDM signal from the DFB laser is coupled, via a variable optical attenuator and an optional 3D positioner, into a 500m 62.5/125μm OM1 MMF having a 3dB optical bandwidth of about 675MHz·km and a linear loss of 0.6dB/km. An optical attenuator is used to control the optical power launched into the MMF link.

At the receiver, the OOFDM signal is detected using a 20GHz PIN with TIA. The PIN has a receiver sensitivity of −17dBm (corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}). The optical-to-electrical converted signal is first amplified with a 2.5GHz, 20dB RF amplifier, then attenuated as necessary to optimise the signal amplitude to suit the ADC's input range. This adjustment also provides electrical gain control to compensate for optical signal attenuation. After passing through an electrical low-pass filter with a 3-dB

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bandwidth of 2.4GHz, the signal is converted via a balun to a differential signal and then digitized by a 4GS/s, 8-bit ADC in the receiver. It should be noted that, the bandwidths of the RF amplifier and the low-pass filter are larger than that corresponding to the OOFDM signal (2GHz for the 4GS/s ADC/DAC). Therefore, these two electrical components do not introduce significant spectral distortions into the OOFDM signal. The system frequency response roll-off effect observed in Fig. 6 and Fig. 9, is mainly due to the DAC employed in the transmitter.

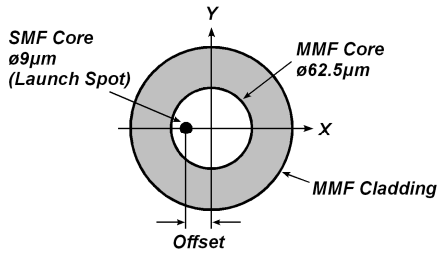

Fig. 4. Launch offset

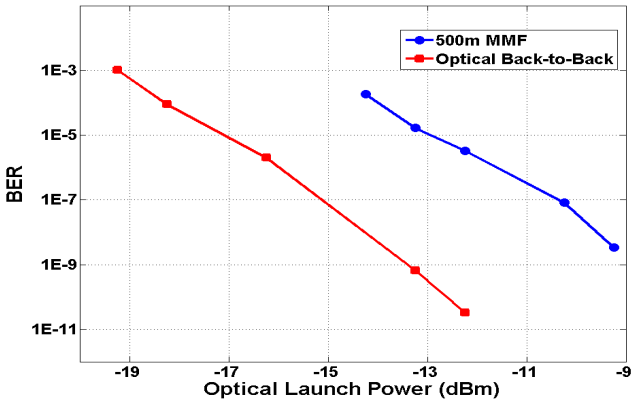

Fig. 5. BER performance of 3Gb/s DQPSK-encoded OOFDM signal transmission over a 500m MMF.

To examine performance robustness to different offset launch conditions, the optical signal from the DFB laser can be coupled into the MMF via a 3D positioner, which enables the fine adjustment of position of laser launch spot to emulate different launch offsets. The definition of the offset can be found in Fig. 4. As a reference point, the central launch position is identified first by adjusting the position of the laser launch spot in the X and Y dimensions until the optical power received at the far end of the MMF is maximised with the corresponding offset ranges being symmetrical and maximized in both the X and Y dimensions. For the MMF adopted in the experiments, the maximum offset range without affecting significantly the output optical power is about ± 25μm.

4. Experimental results

4.1. DQPSK-encoded OOFDM transmission performance

Experimental measurements are first performed of the transmission performance of 3Gb/s DQPSK-encoded OOFDM signals in an IMDD 500m MMF system involving the DML, as shown in Fig. 3. The measured BER as a function of optical launch power is plotted in Fig. 5 for cases of optical back-to-back and 500m MMF transmission. The FPGAs operate at a clock

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speed of 100MHz, and the sample rates of the DAC/ADC are 4GS/s. The DFB bias current is set to 38mA. A 1m mode conditioning patch chord is used to couple the optical signal into the MMF transmission system.

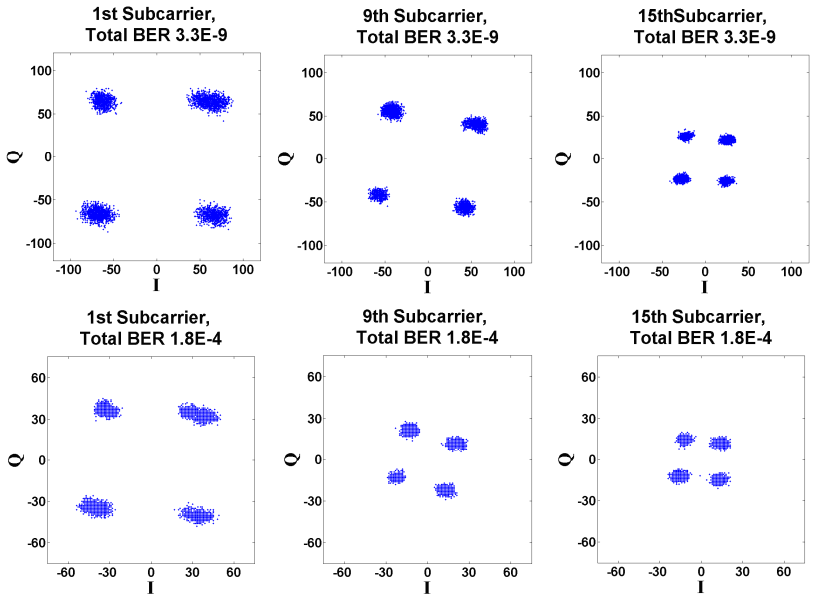

Fig. 6. Constellations of various DQPSK-encoded subcarriers for 3Gb/s signals after transmitting through the 500m MMF.

It can be seen from Fig. 5 that, for the case of 500m MMF transmission (optical back-to-back), a BER as low as $3.3\text{x}10^{-9}$ ($3.3\text{x}10^{-11}$) is achieved at optical launch powers of >-9.2dBm (>-12dBm). In particular, for both cases there is no error floor observed within the BER ranges of practical interest. Taking into account the total linear link loss of about 1dB, an optical power penalty of approximately 3dB at a BER of $1.0\text{x}10^{-4}$ can be obtained from Fig. 5. This penalty mainly results from the MMF-induced differential mode delay (DMD) effect [12].

After transmitting through the 500m MMF, the constellations of the 1st, 9th and 15th subcarriers are presented in Fig. 6 for two representative BERs of $3.3\text{x}10^{-9}$ and $1.8\text{x}10^{-4}$. As seen in Fig. 6, the subcarrier amplitude decreases rapidly for subcarriers locating at high frequencies. The roll-off effect is mainly due to the analogue electrical components (DAC) involved in the transceiver, as very similar behaviour also occurs for an analogue electrical back-to-back case where the electrical signal from the attenuator in the transmitter is directly linked to the low-pass filter in the receiver without any optical components being involved.

4.2. Performance robustness to different offset launch conditions

Experimental explorations are also undertaken of performance robustness to different offset launch conditions. The transmission link configuration and the transceiver parameters are identical to those used in obtaining Fig. 5, except that a 3D positioner is utilised here, as shown in Fig. 3. For 3Gb/s transmission of DQPSK-encoded OOFDM signals over the 500m MMF, the measured BER versus launch offset is given in Fig. 7, in which the variation of the corresponding optical launch power at the input facet of the MMF link is also presented. Figure 7 shows excellent performance robustness with BERs of $<1.0\text{x}10^{-5}$ being maintained over the entire launch offset range from −25μm to 25μm. In particular, as expected, an improved BER performance occurs at the conventional offset launch region (around ± 20μm) [13]. The results imply that the adopted cyclic prefix is sufficiently longer than DMDs associated with different launch offsets [14]. It is also expected that both the performance

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robustness and the corresponding transmission capacity can be improved further if use is made of adaptive modulation on different subcarriers within an OOFDM symbol [14].

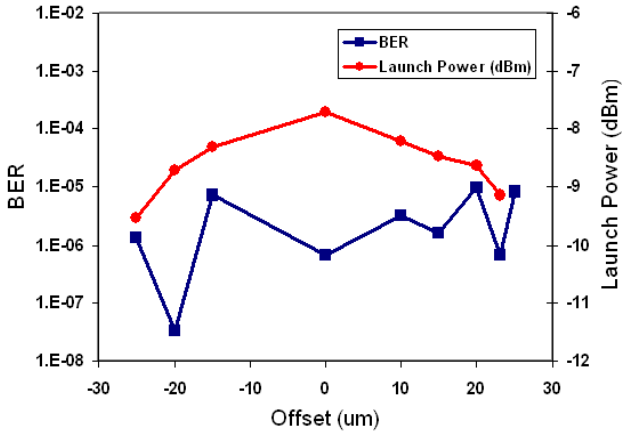

Fig. 7. BER and optical launch power versus launch offset for 3Gb/s over 500m MMF transmission of DQPSK-encoded OOFDM signals.

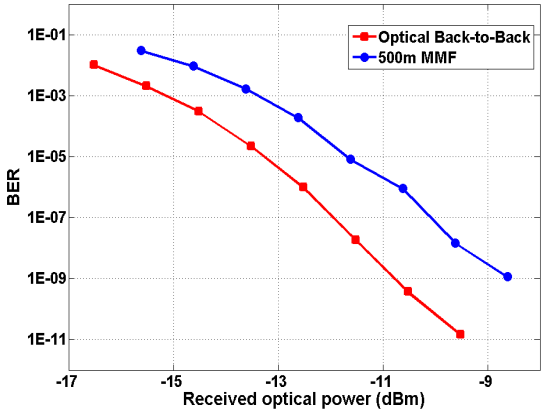

Fig. 8. BER performance for 16-QAM encoded 3Gb/s OOFDM signal transmission over a 500m MMF.

4.3. 16-QAM-encoded OOFDM transmission performance

With the FPGAs' operating speeds and the sample rates of the DAC/ADC being set at 50MHz and 2GS/s, respectively, as well as incorporating the channel estimation technique in the OOFDM transceiver design, a 3Gb/s OOFDM signal can be produced when 16-QAM is taken on all the 15 data-carrying subcarriers. The explorations of the transmission performance of the 16-QAM-encoded 3Gb/s OOFDM signal over the transmission system identical to that used in obtaining Fig. 5, not only enable us to evaluate thoroughly the transceiver design, but also provide an excellent opportunity for comparing the transmission performance of different modulation format-encoded OOFDM signals for achieving the signal bit rate of 3Gb/s.

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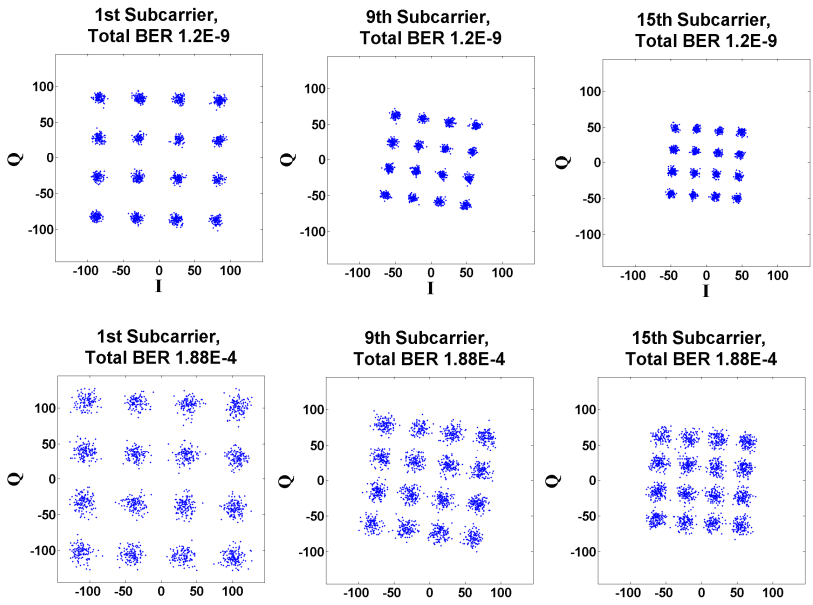

Fig. 9. Constellations of 16-QAM-encoded subcarriers for 3Gb/s OOFDM signals after transmitting through a 500m MMF.

For the above-mentioned transmission system scenario, the measured BER versus received optical power is shown in Fig. 8, in obtaining which, the DFB bias current is set to 36mA. It is shown in Fig. 8 that for received optical powers of >-8.6dBm (>-9.5dBm), BERs lower than $1.2\text{x}10^{-9}$ ($1.5\text{x}10^{-11}$) are measured for 500m MMF transmission (optical back-to-back), and that no error floor is observed. As optical back-to-back systems at low received optical power regions are additive white Gaussian noise (AWGN)-limited, comparisons of optical back-to-back performances between Fig. 8 and Fig. 5 show that, for achieving a BER of $1.0\text{x}10^{-4}$, a 3.7dB increase in optical power is required if DQPSK is replaced by 16-QAM. This is in excellent agreement with theoretical predictions published previously [15]. In addition, Fig. 8 also shows a power penalty of approximately 2dB at a BER of $1.0\text{x}10^{-4}$, which is lower than that shown in Fig. 5. The physics underpinning such a difference is that, the cyclic prefix duration corresponding to the 3Gb/s 16-QAM-encoded signal is doubled in comparison with that corresponding to the 3Gb/s DQPSK-encoded signal. This provides a better compensation of the DMD effect. In addition, compared to the DQPSK-encoded signal, the transmission bandwidth associated with the 16-QAM-encoded signal is halved. As a direct result, it can be seen from Fig. 9 that the roll-off effect is not as significant as those observed in Fig. 6. Similar to Fig. 6, Fig. 9 presents the constellations of the 1st, 9th and 15th subcarriers prior to channel equalization for two representative BERs of $1.2\text{x}10^{-9}$ and $1.88\text{x}10^{-4}$ after transmitting through the 500m MMF.

5. Conclusion

Real-time OOFDM transceivers based on off-the-shelf components including FPGAs, DACs and ADCs have been experimentally demonstrated successfully at 3Gb/s transmission, for the first time, utilising self-developed IFFT/FFT logic algorithms verified at 10Gb/s. The developed transceivers also incorporate a number of key functionalities including live transceiver optimisation and advanced channel estimation. The fastest ever real-time end-to-end transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m MMFs has been achieved with BERs of $<3.3\text{x}10^{-9}$ in DML-based IMDD systems. In addition, excellent performance robustness has also been observed to various offset launch conditions. This work is a significant breakthrough in demonstrating the great potential of the OOFDM technique for practical implementation in optical networks of various architectures.

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Considering the FPGA-based DSP nature of the real-time OOFDM transceiver, extensive research is currently being undertaken in our research group to further improve the transceiver design and performance, and new exciting results are appearing. It is strongly envisaged that a significant increase in transmission capacity may be achieved in the near future, which will be reported elsewhere in due course. In addition, it is estimated that the cost of a DFB-based intensity modulator takes a majority of the total cost of a real-time OOFDM transceiver. For cost-sensitive application scenarios, it is, therefore, greatly beneficial if use can be made of very cheap intensity modulators such as vertical cavity surface emitting lasers (VCSELs) and reflective semiconductor optical amplifiers (RSOAs), real-time OOFDM transceiver performance using these low cost intensity modulators is therefore also to be investigated.

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